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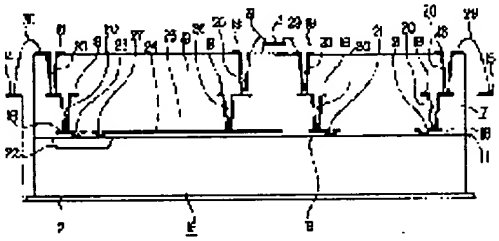
(54) SEMICONDUCTOR DEVICE

(57)Abstract:
PURPOSE: To improve reliability in a multi-chip module wherein a plurality of LSI chips are mounted on an Si substrate so as to contain wirings.
CONSTITUTION: In the case of manufacturing a multilayer wiring board 11, an N-type diffusion layer 22 is formed in the interface part to a thin film wiring board 17 in an Si wafer substrate 16. A PN junction protective diode is formed between the N-type diffusion layer 22 and the P-type Si wafer substrate 16. An instantaneously applied voltage across a metal electrode 25 and the Si wafer substrate 16 can be limited by the protective diode. Hence a decoupling capacitor 24 for reducing power supply noise caused by fluctuation of the consumption current of an LSI chip 13 can be protected from being broken down by high voltage noise from the outside.



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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to semiconductor devices, such as a multi chip module which comes to carry two or more LSI chips on (Silicon Si) substrate including wiring.
[0002]
[Description of the Prior Art] The time delay produced according to a spatial distance between LSI (Large Scale Integrated Circuit) has been a problem with improvement in the speed of a computer or communication equipment, and it is becoming impossible in recent years, to demonstrate performance sufficient by the method of carrying out the packaging of each LSI chip, and mounting on a printed circuit board.
[0003] The multi chip module (MCM) which mounted two or more LSI bare chips on the multilayer-interconnection substrate as one of the methods of solving this problem is known.
[0004] Drawing 8 shows an example of the conventional MCM roughly.
[0005] The thin film wiring substrate 104, for example, the multilayer-interconnection substrate which comes to carry out the laminating of the silicon oxidization (SiO2) film 103 with which between two or more metal wiring layers 102 which consist of aluminum (aluminum), and the wiring layer 102 is insulated, this MCM on the front face of Si wafer substrate 101 The LSI chip which was carried on the bed 105 of a package and was further arranged in the front face of the multilayer-interconnection substrate 104 (for convenience) only one is shown in drawing -- it considers as composition including wiring from the wiring between 106 and the external VDD terminal 107, and the external grand terminal 108 to LSI chip 106 etc.
[0006] That is, the external VDD terminal 107 is electrically connected with the metal electrode 113 of the decoupling capacitor 112 through the VIA hole 111 which connects between the metal wiring layers 102 while connecting with the metal wiring layer 102 on the multilayer-interconnection substrate 104 through a bonding wire 110.
[0007] The decoupling capacitor 112 is formed in order to reduce the power supply noise by change of the consumed electric current of LSI chip 106, and the metal electrode 113 of this capacitor 112 is connected with VDD terminal 106a of LSI chip 106 through the bonding wire 114 through the VIA hole 111 which connects between the metal wiring layers 102.
[0008] In addition, the metal electrode 113 constitutes the power plane and it prevents the inductance of power supply wiring and resistance increasing.
[0009] On the other hand, the external grand terminal 108 is connected with grand terminal 106b of LSI chip 106 through the bonding wire 116 through the VIA hole 111 which connects between a contact hole 115 and the metal wiring layer 102 while connecting with Si wafer substrate 101 electrically through the VIA hole 111 and contact hole 115 which connect between the metal wiring layers 102 for the current supply to LSI chip 106.
[0010] Si wafer substrate 101 has the role of a ground plane, and prevents the inductance of power supply wiring and resistance increasing like the above-mentioned power plane.
[0011] However, in MCM of such composition, the reliability of the decoupling capacitor 112 poses a problem, and when a high-voltage noise was especially added momentarily from the outside, there was a fault which a capacitor 112 destroys of being easy to start the so-called ESD (Electro-Static Destruction).
[0012]
[Problem(s) to be Solved by the Invention] As described above, in the conventional MCM, it was easy to start ESD and there was a fault of a low in reliability.
[0013] Then, this invention can prevent generating of ESD and aims at offering the semiconductor device which can secure high reliability.
[0014]
[Means for Solving the Problem] If it is in the semiconductor device of this invention in order to attain the above-mentioned purpose, it consists of input-protection circuits which restrict the voltage applied to the multilayer-interconnection substrate which carries out the laminating of a thin film wiring layer and the insulating layer to the front face of a semiconductor substrate, and comes to form a thin film wiring substrate in it, the aforementioned semiconductor substrate of this multilayer-interconnection substrate, the aforementioned thin film wiring layer, or the aforementioned insulating layer.
[0015] Moreover, if it is in the semiconductor device of this invention, it consists of input-protection circuits which restrict

the voltage applied to the front face of a semiconductor substrate at the multilayer-interconnection substrate which carries out the laminating of a thin film wiring layer and the insulating layer, and comes to form a thin film wiring substrate, two or more semiconductor chips arranged on this multilayer-interconnection substrate, the capacitor element prepared that the power supply noise by change of the consumed electric current of this semiconductor chip should be reduced, and this capacitor element.

[0016] Furthermore, if it is in the semiconductor device of this invention, it consists of input-protection circuits which restrict the voltage applied to the front face of a semiconductor substrate at the multilayer-interconnection substrate which carries out the laminating of a thin film wiring layer and the insulating layer, and comes to form a thin film wiring substrate, two or more semiconductor chips arranged on this multilayer-interconnection substrate, the semiconductor device prepared that the switching drive of this semiconductor chip should be carried out, and this semiconductor device.

[0017]

[Function] Since it can prevent that the absolute value of the voltage applied to a semiconductor device becomes by the above-mentioned means more than constant value, this invention becomes possible [protecting a semiconductor device from destruction by the high-voltage noise momentarily added from the outside].

[0018]

[Example] Hereafter, the example of this invention is explained with reference to a drawing.

[0019] Drawing 1 shows the structure of MCM concerning the 1st example roughly.

[0020] That is, Book MCM is considered as composition including wiring from the wiring between LSI chips (only one is shown in drawing for convenience) 13 arranged in the front face of the multilayer-interconnection substrate 11 and the external VDD electrode 14, and the external grand electrode 15 to LSI chip 13 etc. while the multilayer-interconnection substrate 11 is carried on the bed 12 of a package.

[0021] The above-mentioned multilayer-interconnection substrate 11 consists of an Si wafer substrate 16 of P type, and a thin film wiring substrate 17 formed in the front face of this Si wafer substrate 16.

[0022] The thin shape wiring substrate 17 carries out the laminating of two or more metal wiring layers 18 which consist of aluminum (aluminum), and the silicon oxidization (SiO2) film 19 with which between this wiring layer 18 is insulated by turns, and is constituted.

[0023] And different metal wiring layer 18 are electrically connected through the VIA hole 20 if needed.

[0024] Moreover, the lowermost metal wiring layer 18 and lowermost Si wafer substrate 16 are electrically connected through the contact hole 21 if needed.

[0025] Here, the N type diffusion layer 22 is alternatively made by the boundary section with the above-mentioned thin film wiring substrate 17 in the above-mentioned Si wafer substrate 16, and the PN-junction protection diode as an input-protection circuit is formed by this N type diffusion layer 22 and Si wafer substrate 16 of P type.

[0026] This N type diffusion layer 22 is electrically connected with the metal wiring layer 18 of the bottom in the above-mentioned thin film wiring substrate 17 through the contact hole 23 if needed.

[0027] Moreover, near the boundary section with the above-mentioned Si wafer substrate 16 in the above-mentioned thin film wiring substrate 17, the decoupling capacitor 24 is formed in order to reduce the power supply noise by change of the consumed electric current of LSI chip 13.

[0028] And the metal electrode 25 of this capacitor 24 is electrically connected with the above-mentioned N type diffusion layer 22 through the contact hole 27 while connecting with the metal wiring layer 18 in the above-mentioned thin film wiring substrate 17 electrically through the VIA hole 26 if needed.

[0029] The above-mentioned external grand electrode 15 is connected by the still more nearly same method as the grand electrode of LSI chip 13, after connecting with Si wafer substrate 16 electrically through a bonding wire 28, the metal wiring layer 18 of the front face of the thin film wiring substrate 17, the VIA hole 20, the metal wiring layer 18 in the thin film wiring substrate 17, the VIA hole 20, the lowermost metal wiring layer 18, and a contact hole 21 for the current supply to LSI chip 13.

[0030] That is, Si wafer substrate 16 is electrically connected to the grand electrode of LSI chip 13 through a contact hole 21, the metal wiring layer 18 of the bottom in the thin film wiring substrate 17, the VIA hole 20, the metal wiring layer 18 in the thin film wiring substrate 17, the VIA hole 20, the metal wiring layer 18 of the front face of the thin film wiring substrate 17, and a bonding wire 29, and supply of the power supply from the above-mentioned external grand electrode 15 to LSI chip 13 is performed.

[0031] In this case, Si wafer substrate 16 constitutes the ground plane, and has played the role which prevents the inductance of power supply wiring and resistance increasing.

[0032] On the other hand, the external VDD electrode 14 is electrically connected to the N type diffusion layer 22 in Si wafer substrate 16 through a bonding wire 30, the metal wiring layer 18 of the front face of the thin film wiring substrate 17, the VIA hole 20, the metal wiring layer 18 in the thin film wiring substrate 17, the VIA hole 20, the lowermost metal wiring layer 18, and the contact hole 23.

[0033] Moreover, similarly, the N type diffusion layer 22 is electrically connected to the VDD electrode of LSI chip 13 through a contact hole 27, the metal electrode 25 of the decoupling capacitor 24, the VIA hole 26, the metal wiring layer 18 in the thin film wiring substrate 17, the VIA hole 20, the metal wiring layer 18 of the front face of the thin film wiring substrate 17, and a bonding wire 31, and supply of the power supply from the above-mentioned external VDD electrode 14 to LSI chip

13 is performed.
[0034] In this case, the metal electrode 25 of the decoupling capacitor 24 constitutes the power plane, and has played the role which prevents the inductance of power supply wiring and resistance increasing.
[0035] In MCM which the decoupling capacitor 24 consisted of between such structure, i.e., a power supply, and the gland, if the noise of the high voltage joins the external VDD electrode 14 when the N type diffusion layer 22 is constituted in the boundary section with the thin film wiring substrate 17 in Si wafer substrate 16, the PN-junction protection diode formed between the N type diffusion layer 22 of Si wafer substrate 16 and Si wafer substrate 16 of P type will be in switch-on.
[0036] Since the voltage added between the metal electrode 25 of the decoupling capacitor 24 and the gland of Si wafer substrate 16 can be reduced by this, when a high-voltage noise is momentarily added from the outside, it can prevent that the so-called ESD (Electro-Static Destruction) which a capacitor 24 destroys happens.
[0037] Similarly, when the noise of the high voltage joins the external grand electrode 15, the PN-junction protection diode formed between the N type diffusion layer 22 of Si wafer substrate 16 and Si wafer substrate 16 of P type will be in switch-on, and can prevent ESD.
[0038] In this case, PN-junction protection diode has a large effect for ESD prevention of the direction which sees from the external VDD electrode 14 and the external grand electrode 15, and is connected to near rather than the decoupling capacitor 24.
[0039] Drawing 2 shows the example of the upper surface side layout of MCM.
[0040] That is, as physical relationship of arrangement, it is most desirable to establish [of the PN-junction protection diode and the decoupling capacitor 24 to the external two electrodes 14 and 15] the N type diffusion layer 22 in the shape of a guard link between the external VDD electrode 14 and the external grand electrode 15, and the decoupling capacitor 24 (specifically metal electrode 25), for example.
[0041] In addition, in this 1st example, it is only forming the N type diffusion layer 22 alternatively on Si wafer substrate 16 of P type beforehand in the case of manufacture of the multilayer-interconnection substrate 11 of MCM, and constituting simply is possible.
[0042] Next, the 2nd example of this invention is explained.
[0043] Drawing 3 shows the structure of MCM concerning the 2nd example roughly.
[0044] That is, Book MCM is considered as composition including wiring from the wiring between LSI chips (only one is shown in drawing for convenience) 13 arranged in the front face of the multilayer-interconnection substrate 11 and the external VDD electrode 14, and the external grand electrode 15 to LSI chip 13 etc. while the multilayer-interconnection substrate 11 is carried on the bed 12 of a package.
[0045] The above-mentioned multilayer-interconnection substrate 11 consists of an Si wafer substrate 16 of P type, and a thin film wiring substrate 17 formed in the front face of this Si wafer substrate 16.
[0046] The thin shape wiring substrate 17 carries out the laminating of two or more metal wiring layers 18 which consist of aluminum (aluminum), and the silicon oxidization (SiO2) film 19 with which between this wiring layer 18 is insulated by turns, and is constituted.
[0047] And different metal wiring layer 18 are electrically connected through the VIA hole 20 if needed.
[0048] Moreover, the lowermost metal wiring layer 18 and lowermost Si wafer substrate 16 are electrically connected through the contact hole 21 if needed.
[0049] Here, the N type diffusion layer 22 is alternatively made by the boundary section with the above-mentioned thin film wiring substrate 17 in the above-mentioned Si wafer substrate 16, and the PN-junction protection diode as an input-protection circuit is formed by this N type diffusion layer 22 and Si wafer substrate 16 of P type.
[0050] Moreover, the drain diffusion layer 41 and the source diffusion layer 42 are alternatively made by the boundary section with the above-mentioned thin film wiring substrate 17 in the above-mentioned Si wafer substrate 16, and MOS transistor 43 is formed by both [these] the diffusion layers 41 and 42 and Si wafer substrate 16 of P type.
[0051] And the above-mentioned N type diffusion layer 22 is electrically connected with the gate electrode 44 of above-mentioned MOS transistor 43 through the metal wiring layer 18 and the VIA hole 32 in a contact hole 27, the metal wiring layer 18 of the bottom in the thin film wiring substrate 17, the VIA hole 20, and the thin film wiring substrate 17 while connecting with the metal wiring layer 18 of the bottom in the above-mentioned thin film wiring substrate 17 electrically through a contact hole 23 if needed.
[0052] Furthermore, near the boundary section with the above-mentioned Si wafer substrate 16 in the above-mentioned thin film wiring substrate 17, the decoupling capacitor 24 is formed in order to reduce the power supply noise by change of the consumed electric current of LSI chip 13.
[0053] And the metal electrode 25 of this capacitor 24 is further connected to the VDD electrode of LSI chip 13 electrically through the VIA hole 20, the metal wiring layer 18 of the front face of the thin film wiring substrate 17, and the bonding wire 31 while connecting with the metal wiring layer 18 in the above-mentioned thin film wiring substrate 17 electrically through the VIA hole 26 if needed.
[0054] The above-mentioned external grand electrode 15 is connected by the still more nearly same method as the grand electrode of LSI chip 13, after connecting with Si wafer substrate 16 electrically through a bonding wire 28, the metal wiring layer 18 of the front face of the thin film wiring substrate 17, the VIA hole 20, the metal wiring layer 18 in the thin film wiring substrate 17, the VIA hole 20, the lowermost metal wiring layer 18, and a contact hole 21 for the current supply to LSI chip

13.
[0055] That is, Si wafer substrate 16 is electrically connected to the grand electrode of LSI chip 13 through a contact hole 21, the metal wiring layer 18 of the bottom in the thin film wiring substrate 17, the VIA hole 20, the metal wiring layer 18 in the thin film wiring substrate 17, the VIA hole 20, the metal wiring layer 18 of the front face of the thin film wiring substrate 17, and a bonding wire 29, and supply of the power supply from the above-mentioned external grand electrode 15 to LSI chip 13 is performed.
[0056] In this case, Si wafer substrate 16 constitutes the ground plane, and has played the role which prevents the inductance of power supply wiring and resistance increasing.
[0057] On the other hand, the external VDD electrode 14 is electrically connected also to the gate electrode 44 of MOS transistor 43 like the above while connecting with the N type diffusion layer 22 in Si wafer substrate 16 electrically through a bonding wire 30, the metal wiring layer 18 of the front face of the thin film wiring substrate 17, the VIA hole 20, the metal wiring layer 18 in the thin film wiring substrate 17, the VIA hole 20, the lowermost metal wiring layer 18, and the contact hole 23.
[0058] In MCM which the decoupling capacitor 24 consisted of between such structure, i.e., a power supply, and the gland, if the noise of the high voltage joins the external VDD electrode 14 when the N type diffusion layer 22 and MOS transistor 43 are constituted in the boundary section with the thin film wiring substrate 17 in Si wafer substrate 16, the PN-junction protection diode formed between the N type diffusion layer 22 of Si wafer substrate 16 and Si wafer substrate 16 of P type will be in switch-on.
[0059] Since the voltage which joins the gate electrode 44 of MOS transistor 43 momentarily by this can be reduced, when a high-voltage noise is momentarily added from the outside, it can prevent that the so-called ESD which the gate insulator layer 45 of MOS transistor 43 destroys happens.
[0060] In addition, in this 2nd example, it is only forming the N type diffusion layer 22 and MOS transistor 43 alternatively on Si wafer substrate 16 of P type beforehand in the case of manufacture of the multilayer-interconnection substrate 11 of MCM, and constituting simply is possible.
[0061] Next, the 3rd example of this invention is explained.
[0062] Drawing 4 shows the structure of MCM concerning the 3rd example roughly.
[0063] That is, Book MCM is considered as composition including wiring from the wiring between LSI chips (only one is shown in drawing for convenience) 13 arranged in the front face of the multilayer-interconnection substrate 11 and the external VDD electrode 14, and the external grand electrode 15 to LSI chip 13 etc. while the multilayer-interconnection substrate 11 is carried on the bed 12 of a package.
[0064] The above-mentioned multilayer-interconnection substrate 11 consists of an Si wafer substrate 16 of P type, and a thin film wiring substrate 17 formed in the front face of this Si wafer substrate 16.
[0065] The thin shape wiring substrate 17 carries out the laminating of two or more metal wiring layers 18 which consist of aluminum (aluminum), and the silicon oxidization (SiO2) film 19 with which between this wiring layer 18 is insulated by turns, and is constituted.
[0066] And different metal wiring layer 18 are electrically connected through the VIA hole 20 if needed.
[0067] Moreover, the lowermost metal wiring layer 18 and lowermost Si wafer substrate 16 are electrically connected through the contact hole 21 if needed.
[0068] Here, the drain diffusion layer 41 and the source diffusion layer 42 are alternatively made by the boundary section with the above-mentioned thin film wiring substrate 17 in the above-mentioned Si wafer substrate 16, and MOS transistor 43 as an input-protection circuit is formed by both [these] the diffusion layers 41 and 42 and Si wafer substrate 16 of P type.
[0069] And the drain diffusion layer 41 of MOS transistor 43 is electrically connected with the metal electrode 25 of the decoupling capacitor 24 mentioned later through the metal wiring layer 53 shown with an illustration dashed line while connecting with the gate electrode 44 of MOS transistor 43 electrically through the metal wiring layer 18 and the VIA hole 52 of the bottom of a contact hole 51 and the thin film wiring substrate 17.
[0070] Moreover, the gate electrode 44 of above-mentioned MOS transistor 43 is electrically connected with the metal wiring layer 18 of the thin film wiring substrate 17 through the VIA hole 54 if needed.
[0071] Furthermore, near the boundary section with the above-mentioned Si wafer substrate 16 in the above-mentioned thin film wiring substrate 17, the decoupling capacitor 24 is formed in order to reduce the power supply noise by change of the consumed electric current of LSI chip 13.
[0072] And the metal electrode 25 of this capacitor 24 is electrically connected to the VDD electrode of LSI chip 13 through the VIA hole 26, the metal wiring layer 18 in the above-mentioned thin film wiring substrate 17, the VIA hole 20, the metal wiring layer 18 of the front face of the thin film wiring substrate 17, and the bonding wire 31 while connecting with the above-mentioned drain diffusion layer 41 of MOS transistor 43 if needed.
[0073] The above-mentioned external grand electrode 15 is connected by the still more nearly same method as the grand electrode of LSI chip 13, after connecting with Si wafer substrate 16 electrically through a bonding wire 28, the metal wiring layer 18 of the front face of the thin film wiring substrate 17, the VIA hole 20, the metal wiring layer 18 in the thin film wiring substrate 17, the VIA hole 20, the lowermost metal wiring layer 18, and a contact hole 21 for the current supply to LSI chip 13.
[0074] That is, Si wafer substrate 16 is electrically connected to the grand electrode of LSI chip 13 through a contact hole 21,

the metal wiring layer 18 of the bottom in the thin film wiring substrate 17, the VIA hole 20, the metal wiring layer 18 in the thin film wiring substrate 17, the VIA hole 20, the metal wiring layer 18 of the front face of the thin film wiring substrate 17, and a bonding wire 29, and supply of the power supply from the above-mentioned external grand electrode 15 to LSI chip 13 is performed.

[0075] In this case, Si wafer substrate 16 constitutes the ground plane, and has played the role which prevents the inductance of power supply wiring and resistance increasing.

[0076] On the other hand, the external VDD electrode 14 is electrically connected to the drain diffusion layer 41 of MOS transistor 43 in Si wafer substrate 16 through a bonding wire 30, the metal wiring layer 18 of the front face of the thin film wiring substrate 17, the VIA hole 20, the metal wiring layer 18 in the thin film wiring substrate 17, the VIA hole 54, the gate electrode 44 of MOS transistor 43, the VIA hole 52, the lowermost metal wiring layer 18, and the contact hole 51.

[0077] Moreover, the external VDD electrode 14 is electrically connected also to the metal electrode 25 of the decoupling capacitor 24 through the drain diffusion layer 41 of above-mentioned MOS transistor 43 like ****.

[0078] And supply of the power supply from the above-mentioned external VDD electrode 14 to LSI chip 13 is performed by connecting the metal electrode 25 of the decoupling capacitor 24 to the VDD electrode of LSI chip 13 electrically like ****.

[0079] In this case, the metal electrode 25 of the decoupling capacitor 24 constitutes the power plane, and has played the role which prevents the inductance of power supply wiring and resistance increasing.

[0080] In MCM which the decoupling capacitor 24 consisted of between such structure, i.e., a power supply, and the gland, if the noise of the high voltage joins the external VDD electrode 14 when MOS transistor 43 is constituted in the boundary section with the thin film wiring substrate 17 in Si wafer substrate 16, MOS transistor 43 will be in an ON state.

[0081] Since the voltage momentarily added by this between the metal electrode 25 of the decoupling capacitor 24 and the gland of Si wafer substrate 16 can be reduced, when a high-voltage noise is momentarily added from the outside, it can prevent that the so-called ESD which a capacitor 24 destroys happens.

[0082] In addition, in this 3rd example, it is only forming MOS transistor 43 alternatively on Si wafer substrate 16 of P type beforehand in the case of manufacture of the multilayer-interconnection substrate 11 of MCM, and constituting simply is possible.

[0083] However, in this case, it is larger than the thickness of the insulator layer of KYABASHITA 24 in the thickness of the gate insulator layer 45 of MOS transistor 43, and it is required to make pressure-proofing high moreover.

[0084] Next, the 4th example of this invention is explained.

[0085] Drawing 5 shows the structure of MCM concerning the 4th example roughly.

[0086] That is, Book MCM is considered as composition including wiring from the wiring between LSI chips (only one is shown in drawing for convenience) 13 arranged in the front face of the multilayer-interconnection substrate 11 and the external VDD electrode 14, and the external grand electrode 15 to LSI chip 13 etc. while the multilayer-interconnection substrate 11 is carried on the bed 12 of a package.

[0087] The above-mentioned multilayer-interconnection substrate 11 consists of a low-concentration epitaxial growth phase 61 and a thin film wiring substrate 17 formed of deposition on this epitaxial growth phase 61 rather than it which was formed in the front face of Si wafer substrate (high concentration) 16 of P type, and this Si wafer substrate 16.

[0088] The thin shape wiring substrate 17 carries out the laminating of two or more metal wiring layers 18 which consist of aluminum (aluminum), and the silicon oxidization (SiO2) film 19 with which between this wiring layer 18 is insulated by turns, and is constituted.

[0089] And different metal wiring layer 18 are electrically connected through the VIA hole 20 if needed.

[0090] Moreover, the lowermost metal wiring layer 18 is electrically connected with high concentration P type diffusion layer 61a in the epitaxial growth phase 61 through the contact hole 21 if needed.

[0091] Here, the drain diffusion layer 41 and the source diffusion layer 42 are alternatively made by the boundary section with the above-mentioned thin film wiring substrate 17 in the above-mentioned epitaxial growth phase 61, and MOS transistor (aluminum gate) 43 is formed by these drain diffusion layer 41 and the source diffusion layer 42, and the epitaxial growth phase 61.

[0092] The drain diffusion layer 41 of this MOS transistor 43 is connected with the poly Si gate electrode 74 of poly Si gate MOS transistor 73 mentioned later through the metal wiring layer 63 shown with an illustration dashed line while connecting with the gate electrode 44 through a contact hole 62 if needed.

[0093] Moreover, the source diffusion layer 42 of MOS transistor 43 is electrically connected with high concentration P type diffusion layer 61a of the epitaxial growth phase 61 through the contact hole 64, the metal wiring layer 18 of the bottom in the thin film wiring substrate 17, and the contact hole 65 if needed.

[0094] The drain diffusion layer 71 and the source diffusion layer 72 are alternatively made by the boundary section with the above-mentioned thin film wiring substrate 17 in the above-mentioned epitaxial growth phase 61, and poly Si gate MOS transistor 73 is formed by these drain diffusion layer 71 and the source diffusion layer 72, and the epitaxial growth phase 61.

[0095] Near the boundary section with the above-mentioned epitaxial growth phase 61 in the above-mentioned thin film wiring substrate 17, the decoupling capacitor 24 is formed in order to reduce the power supply noise by change of the consumed electric current of LSI chip 13.

[0096] And the metal electrode 25 of this capacitor 24 is further connected to the VDD electrode of the aforementioned semiconductor chip 13 electrically through the VIA hole 20, the metal wiring layer 18 of the front face of the

above-mentioned thin film wiring substrate 17, and the bonding wire 31 while connecting with the metal wiring layer 18 in the above-mentioned thin film wiring substrate 17 electrically through the VIA hole 26 if needed.
[0097] The above-mentioned external grand electrode 15 The current supply to LSI chip 13 sake, Pass a bonding wire 28, the metal wiring layer 18 of the front face of the thin film wiring substrate 17, the VIA hole 20, the metal wiring layer 18 in the thin film wiring substrate 17, the VIA hole 20, the lowermost metal wiring layer 18, and a contact hole 21. While connecting with high concentration P type diffusion layer 61a of the epitaxial growth phase 61 electrically, it connects with Si wafer substrate 16 electrically through this high concentration P type diffusion layer 61a.
[0098] By and the still more nearly same method as the grand electrode of LSI chip 13 Si wafer substrate 16 That is, high concentration P type diffusion layer 61a of the epitaxial growth phase 61, Pass a contact hole 21, the metal wiring layer 18 of the bottom in the thin film wiring substrate 17, the VIA hole 20, the metal wiring layer 18 in the thin film wiring substrate 17, the VIA hole 20, the metal wiring layer 18 of the front face of the thin film wiring substrate 17, and a bonding wire 29. It connects with the grand electrode of LSI chip 13 electrically, and supply of the power supply from the above-mentioned external grand electrode 15 to LSI chip 13 is performed.
[0099] In this case, Si wafer substrate 16 constitutes the ground plane, and has played the role which prevents the inductance of power supply wiring and resistance increasing.
[0100] On the other hand, the external VDD electrode 14 is electrically connected to the drain diffusion layer 41 of MOS transistor 43 formed in the epitaxial growth phase 61 through a bonding wire 30, the metal wiring layer 18 of the front face of the thin film wiring substrate 17, the VIA hole 20, the metal wiring layer 18 in the thin film wiring substrate 17, the VIA hole 54, the gate electrode 44 of MOS transistor 43, and the contact hole 62.
[0101] Moreover, the external VDD electrode 14 is electrically connected also to the poly Si gate electrode 74 of poly Si gate MOS transistor 73 through the drain diffusion layer 41 of above-mentioned MOS transistor 43 like ****.
[0102] In MCM which the decoupling capacitor 24 consisted of between such structure, i.e., a power supply, and the gland, if the noise of the high voltage joins the external VDD electrode 14 when MOS transistors 43 and 73 are constituted in the boundary section with the thin film wiring substrate 17 in the epitaxial growth phase 61, MOS transistor 43 will be in an ON state.
[0103] Since the voltage which joins momentarily the poly Si gate electrode 74 of poly Si gate MOS transistor 73 by this can be reduced, when a high-voltage noise is momentarily added from the outside, it can prevent that the so-called ESD which poly Si gate MOS transistor 73 destroys happens.
[0104] In addition, in this 4th example, it is possible to only add each process which forms the epitaxial growth phase 61, MOS transistor 43, and poly Si gate MOS transistor 73 alternatively on Si wafer substrate 16 of P type beforehand in the case of manufacture of the multilayer-interconnection substrate 11 of MCM, and to constitute simply.
[0105] And since it is possible to lower the concentration of the epitaxial growth phase 61 in the case of this example, poly Si gate MOS transistor 73 functions as a switching element, that is, can control the threshold voltage of MOS transistor 73 to a small value.
[0106] Next, the 5th example of this invention is explained.
[0107] Drawing 6 shows the structure of MCM concerning the 5th example roughly.
[0108] That is, Book MCM is considered as composition including wiring from the wiring between LSI chips (only one is shown in drawing for convenience) 13 arranged in the front face of the multilayer-interconnection substrate 11 and the external VDD electrode 14, and the external grand electrode 15 to LSI chip 13 etc. while the multilayer-interconnection substrate 11 is carried on the bed 12 of a package.
[0109] The above-mentioned multilayer-interconnection substrate 11 consists of an Si wafer substrate 16 of P type, and a thin film wiring substrate 17 formed in the front face of this Si wafer substrate 16.
[0110] Near the boundary section with the above-mentioned Si wafer substrate 16, it is the purpose which reduces the power supply noise by change of the consumed electric current of LSI chip 13, and the thin shape wiring substrate 17 has the decoupling capacitor 81 which consists of an up metal electrode 82 and a lower metal electrode 83, and is constituted while carrying out the laminating of two or more metal wiring layers 18 which consist of aluminum (aluminum), and the silicon oxidization (SiO2) film 19 with which between this wiring layer 18 is insulated by turns.
[0111] And different metal wiring layer 18 are electrically connected through the VIA hole 20 if needed.
[0112] Moreover, the lowermost metal wiring layer 18 is electrically connected with the lower metal electrode 83 of the above-mentioned decoupling capacitor 81 through the contact hole 84 if needed.
[0113] Furthermore, the lower metal electrode 83 of this decoupling capacitor 81 is electrically connected with the above-mentioned Si wafer substrate 16 through the contact hole 85 if needed.
[0114] Here, the N type diffusion layer 22 is alternatively made by the boundary section with the above-mentioned thin film wiring substrate 17 in the above-mentioned Si wafer substrate 16, and the PN-junction protection diode as an input-protection circuit is formed by this N type diffusion layer 22 and Si wafer substrate 16 of P type.
[0115] This N type diffusion layer 22 is electrically connected with the up metal electrode 82 of the above-mentioned decoupling capacitor 81 through the lowermost metal wiring layer 18 and the lowermost VIA hole 87 in a contact hole 86 and the above-mentioned thin film wiring substrate 17 while connecting with the metal wiring layer 18 of the bottom in the above-mentioned thin film wiring substrate 17 electrically through a contact hole 23 if needed.
[0116] And the up metal electrode 82 of this capacitor 81 is electrically connected with the metal wiring layer 18 in the

above-mentioned thin film wiring substrate 17 through the VIA hole 88 if needed.
[0117] The above-mentioned external grand electrode 15 The current supply to LSI chip 13 sake, A bonding wire 28, the metal wiring layer 18 of the front face of the thin film wiring substrate 17, the VIA hole 20, the metal wiring layer 18 in the thin film wiring substrate 17, the VIA hole 20, the lowermost metal wiring layer 18, the VIA hole 84, the lower metal electrode 83 of the decoupling capacitor 81, And while connecting with Si wafer substrate 16 electrically through a contact hole 85, it connects by the still more nearly same method also as the grand electrode of LSI chip 13.
[0118] Namely, the lower metal electrode 83 of the decoupling capacitor 81 Pass the VIA hole 84, the metal wiring layer 18 of the bottom in the thin film wiring substrate 17, the VIA hole 20, the metal wiring layer 18 in the thin film wiring substrate 17, the VIA hole 20, the metal wiring layer 18 of the front face of the thin film wiring substrate 17, and a bonding wire 29. It connects with the grand electrode of LSI chip 13 electrically, and supply of the power supply from the above-mentioned external grand electrode 15 to LSI chip 13 is performed.
[0119] In this case, the lower metal electrode 83 of the decoupling capacitor 81 constitutes the ground plane, and has played the role which prevents the inductance of power supply wiring and resistance increasing.
[0120] On the other hand, the external VDD electrode 14 is electrically connected to the N type diffusion layer 22 in Si wafer substrate 16 through a bonding wire 30, the metal wiring layer 18 of the front face of the thin film wiring substrate 17, the VIA hole 20, the metal wiring layer 18 in the thin film wiring substrate 17, the VIA hole 20, the lower metal wiring layer 18, the VIA hole 20, the lowermost metal wiring layer 18, and the contact hole 23.
[0121] It is made the same. moreover, the N type diffusion layer 22 A contact hole 86, the metal wiring layer 18 of the bottom of the thin film wiring substrate 17, the VIA hole 87, the up metal electrode 82 of the decoupling capacitor 81, the VIA hole 88, the metal wiring layer 18 in the thin film wiring substrate 17, the VIA hole 20, the metal wiring layer 18 of the front face of the thin film wiring substrate 17, And through a bonding wire 31, it connects with the VDD electrode of LSI chip 13 electrically, and supply of the power supply from the above-mentioned external VDD electrode 14 to LSI chip 13 is performed.
[0122] In this case, the up metal electrode 82 of the decoupling capacitor 81 constitutes the power plane, and has played the role which prevents the inductance of power supply wiring and resistance increasing.
[0123] In MCM which the decoupling capacitor 81 consisted of between such structure, i.e., a power supply, and the gland, if the noise of the high voltage joins the external VDD electrode 14 when the N type diffusion layer 22 is constituted in the boundary section with the thin film wiring substrate 17 in Si wafer substrate 16, the PN-junction protection diode formed between the N type diffusion layer 22 of Si wafer substrate 16 and Si wafer substrate 16 of P type will be in switch-on.
[0124] Since the voltage momentarily added by this between the up metal electrode 82 of the decoupling capacitor 81 and the lower metal electrode 83 can be reduced, when a high-voltage noise is momentarily added from the outside, it can prevent that the so-called ESD which a capacitor 81 destroys happens.
[0125] In this case, since the lower metal electrode 83 constitutes the ground plane, compared with the 1st previous example, resistance can be small, can end and can reduce the part and power supply wiring resistance.
[0126] In addition, in this 5th example, it is possible to only add each process which forms the contact hole 86 for connection with the N type diffusion layer 22 and the up metal electrode 82 of the decoupling capacitor 81 alternatively on Si wafer substrate 16 of P type beforehand in the case of manufacture of the multilayer-interconnection substrate 11 of MCM, and to constitute simply.
[0127] Next, the 6th example of this invention is explained.
[0128] Drawing 7 shows the structure of MCM concerning the 6th example roughly.
[0129] That is, Book MCM is considered as composition including wiring from the wiring between LSI chips (only one is shown in drawing for convenience) 13 arranged in the front face of the multilayer-interconnection substrate 11 and the external VDD electrode 14, and the external grand electrode 15 to LSI chip 13 etc. while the multilayer-interconnection substrate 11 is carried on the bed 12 of a package.
[0130] The above-mentioned multilayer-interconnection substrate 11 consists of an Si wafer substrate 16 of P type, and a thin film wiring substrate 17 formed in the front face of this Si wafer substrate 16.
[0131] Near the boundary section with the above-mentioned Si wafer substrate 16, it is the purpose which reduces the power supply noise by change of the consumed electric current of LSI chip 13, and the thin shape wiring substrate 17 has the decoupling capacitor 81 which consists of an up metal electrode 82 and a lower metal electrode 83, and is constituted while carrying out the laminating of two or more metal wiring layers 18 which consist of aluminum (aluminum), and the silicon oxidization (SiO2) film 19 with which between this wiring layer 18 is insulated by turns.
[0132] And different metal wiring layer 18 are electrically connected through the VIA hole 20 if needed.
[0133] Moreover, the lowermost metal wiring layer 18 is electrically connected with the lower metal electrode 83 of the above-mentioned decoupling capacitor 81 through the contact hole 84 if needed.
[0134] Here, the N type diffusion layer 22 is alternatively made by the boundary section with the above-mentioned thin film wiring substrate 17 in the above-mentioned Si wafer substrate 16, and the PN-junction protection diode as an input-protection circuit is formed by this N type diffusion layer 22 and Si wafer substrate 16 of P type.
[0135] In this case, simultaneously that is, with formation of the contact hole mentioned later, diffusion formation of the above-mentioned N type diffusion layer 22 is carried out by the self aryne.
[0136] If needed, it connects with the metal wiring layer 18 of the bottom in the above-mentioned thin film wiring substrate

17 electrically through a contact hole 23, and this N type diffusion layer 22 is further connected with the up metal electrode 82 of the above-mentioned decoupling capacitor 81 electrically through the VIA hole 87.
[0137] And the up metal electrode 82 of this capacitor 81 is electrically connected with the metal wiring layer 18 in the above-mentioned thin film wiring substrate 17 through the VIA hole 88 if needed.
[0138] The above-mentioned external grand electrode 15 is connected by the same method also as the grand electrode of LSI chip 13 while connecting with the lower metal electrode 83 of the decoupling capacitor 81 electrically through a bonding wire 28, the metal wiring layer 18 of the front face of the thin film wiring substrate 17, the VIA hole 20, the metal wiring layer 18 in the thin film wiring substrate 17, the VIA hole 20, the lowermost metal wiring layer 18, and the VIA hole 84 for the current supply to LSI chip 13.
[0139] Namely, the lower metal electrode 83 of the decoupling capacitor 81 Pass the VIA hole 84, the metal wiring layer 18 of the bottom in the thin film wiring substrate 17, the VIA hole 20, the metal wiring layer 18 in the thin film wiring substrate 17, the VIA hole 20, the metal wiring layer 18 of the front face of the thin film wiring substrate 17, and a bonding wire 29. It connects with the grand electrode of LSI chip 13 electrically, and supply of the power supply from the above-mentioned external grand electrode 15 to LSI chip 13 is performed.
[0140] In this case, the lower metal electrode 83 of the decoupling capacitor 81 constitutes the ground plane, and has played the role which prevents the inductance of power supply wiring and resistance increasing.
[0141] Moreover, the above-mentioned external grand electrode 15 is electrically connected with the above-mentioned Si wafer substrate 16 through the bonding wire 91.
[0142] On the other hand, the external VDD electrode 14 is electrically connected to the N type diffusion layer 22 in Si wafer substrate 16 through a bonding wire 30, the metal wiring layer 18 of the front face of the thin film wiring substrate 17, the VIA hole 20, the metal wiring layer 18 in the thin film wiring substrate 17, the VIA hole 20, the lower metal wiring layer 18, the VIA hole 20, the lowermost metal wiring layer 18, and the contact hole 23.
[0143] It is made the same. moreover, the N type diffusion layer 22 The above-mentioned contact hole 23, the metal wiring layer 18 of the bottom of the thin film wiring substrate 17, the VIA hole 87, the up metal electrode 82 of the decoupling capacitor 81, the VIA hole 88, the metal wiring layer 18 in the thin film wiring substrate 17, the VIA hole 20, Through the metal wiring layer 18 of the front face of the thin film wiring substrate 17, and a bonding wire 31, it connects with the VDD electrode of LSI chip 13 electrically, and supply of the power supply from the above-mentioned external VDD electrode 14 to LSI chip 13 is performed.
[0144] In this case, the up metal electrode 82 of the decoupling capacitor 81 constitutes the power plane, and has played the role which prevents the inductance of power supply wiring and resistance increasing.
[0145] In MCM which the decoupling capacitor 81 consisted of between such structure, i.e., a power supply, and the gland, if the noise of the high voltage joins the external VDD electrode 14 when the N type diffusion layer 22 is constituted in the boundary section with the thin film wiring substrate 17 in Si wafer substrate 16, the PN-junction protection diode formed between the N type diffusion layer 22 of Si wafer substrate 16 and Si wafer substrate 16 of P type will be in switch-on.
[0146] Since the voltage momentarily added by this between the up metal electrode 82 of the decoupling capacitor 81 and the lower metal electrode 83 can be reduced, when a high-voltage noise is momentarily added from the outside, it can prevent that the so-called ESD which a capacitor 81 destroys happens.
[0147] And since it is made to constitute the N type diffusion layer 22 and a contact hole 23 from a self aryne, compared with the 5th example mentioned above, the one number of steps of the mask in the case of patterning can be lessened.
[0148] However, formation of the metal layer 92 at the rear face of Si wafer substrate 16 for the good electrical installation of the bonding process to a bed 12, and a bed 12 and Si wafer substrate 16 being obtained is needed.
[0149] It enables it to prevent that the absolute value of the voltage applied to a decoupling capacitor or an MOS transistor becomes more than constant value, as described above.
[0150] That is, it enables it to reduce the high voltage momentarily added from the outside by making the diode or the transistor for input protections in MCM. It becomes possible to protect a decoupling capacitor and an MOS transistor from destruction by the high-voltage noise momentarily added from the outside by this. Therefore, generating of ESD can be prevented and it can be referred to as reliable MCM.
[0151] In addition, in the 3 or 4 above-mentioned examples, although the MOS diode was explained to the example, it can carry out similarly for example, not only with this but with a field transistor.
[0152] In addition, of course in the range which does not change the summary of this invention, deformation implementation is variously possible.
[0153]
[Effect of the Invention] As mentioned above, as explained in full detail, according to this invention, generating of ESD can be prevented, and the semiconductor device which can secure high reliability can be offered.

[Translation done.]